REMARKS

Claims 1, 2 and 4-18 are pending. Claims 15-18 are allowed. By this Response, claim 1 is amended, claim 19 is cancelled and claims 20-35 are added. Reconsideration and allowance based on the above-amendments and following remarks are respectfully requested.

Applicant's appreciate the allowance of claims 15-18 and the indication of claims 4 and 5 as containing allowable subject matter.

Priority

The Office Action alleges that a certified copy of the priority document has not been filed. Applicants note however, that a certified copy of the priority document was filed on July 6, 2001. Applicants attach hereto a copy of the letter to the U.S. Patent and Trademark Office filed on July 6, 2001, a copy of the front page of the certified document and our stamped postcard to verify the filing of the certified priority document.

Drawings

The Office Action requires corrected formal drawings in regard to the proposed drawing corrections filed on May 12, 2003 and approved by the Examiner. Applicants hereby attach formal drawings of Figs. 4 and 5 which were filed as corrected drawings on May 12, 2003.

Claim Objection

The Office Action alleges that claim 19 is improperly dependent upon claim 9 by failing to further limit the features of claim 9. In response, claim 19 is cancelled. Accordingly, the objection is moot.

Claim Rejections

The Office Action rejects claims 1, 2 and 11-14 under 35 U.S.C. §102(b) as being anticipated by Kuroda (U.S. Patent No. 5,550,770) and claims 6-10 and 19 under 35 U.S.C. §103(a) as being unpatentable over Kuroda in view of Tannas (U.S. Patent No. 4,169,258) or Anderson (U.S. Patent No. 3,002,182). These rejections are respectfully traversed.

Claim 1, as amended, recites, *inter alia*, arranging said timing sequence to encompass at least two (2) distinct parts, including a read cycle during which charges flowing between said selected bit line and the cells connecting to said bit line as sensed by the sensing circuitry, and a refresh/write cycle during which polarization state (s) in cells connecting with selected word and bit lines are controlled to correspond with a set of predetermined values, where during read/write cycles each unselected cell is 1/3 Vs or greater, where Vs is the voltage across an addressed cell during read, refresh and write cycles.

For reasons of brevity, applicants arguments filed in the Response dated May 12, 2003, are hereby incorporated by reference.

Kuroda teaches an active memory matrix, which is a memory device having the components, such as the capacitors etc, located within the matrix. This is contrary to the present invention in which a passive matrix is claimed. A passive matrix has the components located at the edge of the matrix. Further, in Kuroda's active matrix during read/write cycles each unselected cell is either 0, $V_0/2$ or V_0. See, for example, Figs. 9(a)-9(b), 10(a)-10(b) and Figs. 12-14. Within the system of Kuroda, during read/write cycles each unselected cell is not 1/3 Vs or greater, which is easily seen by the use of 0 Vs during some write operations. In fact, kuroda's system relies upon the voltages of the unselected cells being reset to 0 volts in order to reduce the stress on the capacitors. See column 13, line 35 through column 14, line 3.

Thus, based on the previous arguments submitted and the arguments above in regard to the newly amended claims, applicants respectfully submit that Kuroda fails to teach or suggest each and every feature of claim 1.

Further, Tannas and Anderson fail to make up for the deficiencies of Kuroda. Thus, the combination of Tannas or Anderson with Kuroda fails to teach applicants' claimed combinations. Accordingly, reconsideration and withdrawal of the above noted rejections are respectfully requested.

Applicants note that added independent claim 20 includes, *inter alia*, the feature of using quiescent voltages, particularly that all word and bit lines are latched to at least one quiescent voltage level when the memory device is in a non-addressed state. Applicants respectfully submit that this feature in combination

with the other claim elements, is not found in the prior art. For example, Kuroda relies on an initialization step which includes the switching of the transfer MOSFET. Kuroda further teaches the latching of unselected word lines and data to the fractional voltage. This is illustrated at least by Fig. 2 in which the each unselected word and bit line is latched to the fractional voltage $V_0/2$ and described in column 6, lines 43-50, column 7, lines 40-46 and column 8, lines 20-25.

Kuroda further teaches away from the use of quiescent voltages by the resetting of voltages of unselected word and data lines to 0 volts. At the end of a writing operations the potentials of word and data lines are first set to $V_0/2$ and then to 0 Volts. This is accomplished in Kuroda by an intentionally applied voltage at each of the inputs. See column 13, lines 37-55. Thus an initialization step is necessary in Kuroda. This is contrary to the use of quiescent voltages, which is essentially the voltage when no input voltage is applied. Therefore, the present invention eliminates the need for an initializing step and reduces the power necessary to pull-up an pull-down voltages by use of the quiescent voltage. Thus, the features of claim 20 are also allowable over the prior art and particularly the cited Kuroda reference.

Conclusion

For at least these reasons, it is respectfully submitted that claims 1, 2 and 6-14 are distinguishable over the cited references. Favorable consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings (Reg. No. 48,917) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) respectfully petition(s) for a two (2) month extension of time for filing a reply in connection with the present application, and the required fee of $410.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment(s)